

REMARKS

This is a full and timely response to the non-final Office Action of January 25, 2005. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this Amendment, claims 1, 2, 7, 8, 10, and 23-36 remain pending in this application, and claims 1 and 7 are directly amended herein. Further, claims 33-36 are newly added. It is believed that the foregoing amendments add no new matter to the present application.

Interview Summary

Applicant wishes to express sincere appreciation for the time that Examiner Chat C. Do spent with Applicants' undersigned Agent and Attorney during a telephone discussion on April 11, 2005, regarding the outstanding Office Action. In the telephone conversation, no exhibits were discussed, and claim 1 was discussed with reference to *Knowles* (U.S. Patent No. 6,446,107). In this regard, Applicants' Agent and Attorney suggested that *Knowles* fails to disclose operands that are propagate, kill, and generate (PKG) representations within the meaning of the instant application. Applicants' Agent and Attorney further suggested that, even if it is assumed *arguendo* that *Knowles* discloses PKG representations, *Knowles* fails to disclose a "first carry-save adder" and a "modified carry-save adder" as recited in claim 1. However, the Examiner disagreed, and no agreement was reached.

Response to §102 Rejections

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See, e.g., *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by *Knowles* (U.S. Patent No. 6,446,107). Claim 1 presently reads as follows:

1. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:

circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;

a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set. (Emphasis added).

Applicant respectfully asserts that *Knowles* fails to disclose at least the features of claim 1 highlighted hereinabove. Therefore, the 35 U.S.C. §102 rejection of claim 1 is improper and should be withdrawn.

In rejecting claim 1, it is asserted in the Office Action that “*Knowles* discloses in Figure 3 an apparatus (abstract) for performing the addition of propagate, kill, and generate recoded numbers.” However, there is nothing in *Knowles* to indicate that any of the alleged “propagate, kill, and generate recoded numbers” satisfy the features of claim 1 highlighted above.

For at least the above reasons, Applicant respectfully asserts that *Knowles* fails to disclose each feature of claim 1. Accordingly, the 35 U.S.C. §102 rejection of claim 1 should be withdrawn.

Claims 2, 23-29, 33, and 34

Claim 2 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Knowles* in view of *Miller* (U.S. Patent No. 5,706,323). Further, claims 23-29 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Knowles*, and claims 33 and 34 have been newly added via the amendments set forth herein. Applicant submits that the pending dependent claims 2, 23-29, 33, and 34 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2, 23-29, 33, and 34 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by

Knowles. Claim 7 presently reads as follows:

7. A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:

receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;

logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and

providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two of the bits of the respective coded logical value are set. (Emphasis added).

For at least reasons similar to those set forth hereinabove in the arguments for allowance of claim 1, Applicant respectfully asserts that *Knowles* fails to disclose at least the features of claim 7 highlighted above. Accordingly, the 35 U.S.C. §102 rejection of claim 7 is improper and should be withdrawn.

Claims 8, 10, and 30-32

Claims 8 and 30-32 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Knowles*. Further, claim 10 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Knowles* in view of *Miller*. Applicant submits that the pending dependent claims 8, 10, and 30-32 contain all

features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8, 10, and 30-32 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 35

Claim 35 has been newly added via the amendments set forth herein. Claim 35 presently reads as follows:

35. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:

circuitry configured to receive an operand defining a logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, wherein the logical value, when decoded into a non-PKG form, has a plurality of bits, wherein the kill bit, if at a particular binary value, indicates that none of the bits of the logical value are set, wherein the propagate bit, if at the particular binary value, indicates that only one of the bits of the logical value is set, and wherein the generate bit, if at the particular binary value, indicates that two bits of the logical value are set; and

a carry save adder configured to add the operand in PKG form to a carry bit without decoding the operand from PKG form.

Applicant submits that the cited art fails to disclose or suggest each of the above features of claim 35. Therefore, this claim is allowable.

Claim 36

Claim 36 has been newly added via the amendments set forth herein. Applicant submits that the pending dependent claim 36 contains all features of its independent claim 35. Since claim 35 should be allowed, as argued hereinabove, pending dependent claim 36 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).


CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**

By:



Jon E. Holland
Reg. No. 41,077
(256) 704-3900 Ext. 103

Hewlett-Packard Development Company, L.P.
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400